Introduction

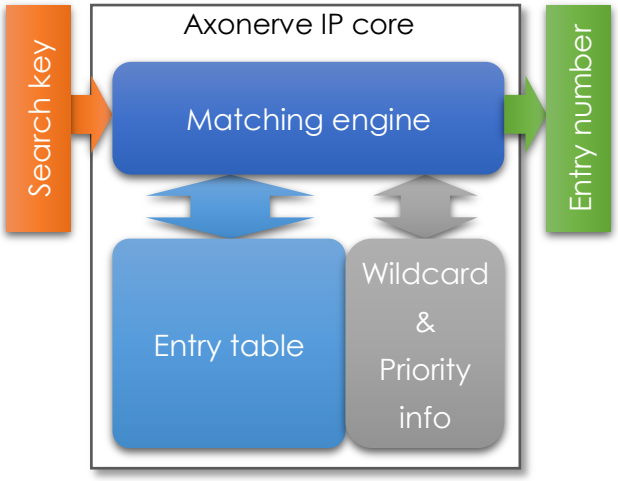
Axonerve is a next generation variant of the content-addressable memory (CAM) solution. Its unique algorithmic matching engine realizes high-speed & low-latency content matching at ultra-low power consumption.

Axonerve can perform continuous search operation with extremely low latency and achieve 150MSPS to track 100Gbps network packets. It can support exact and wildcard matching for N-tuple header fields. It also provides a priority function that determines which one should be finally selected out of multiple matches. You don't need to sort or update a whole entry table any more to change the matching order.

Axonerve is a fully-synthesizable IP core. It adopts common 6T-SRAM technology and requires no special memory structure design. It leads to power and area saving, and enables you to implement single or multiple instances of Axonerve IP cores in FPGA as well as ASIC.

Applications

- SDN/OpenFlow switch
- L2 MAC lookup
- Deep packet inspection
- Carrier grade NAT
- Memcached server
- Dedup storage
- Virus signature matching
- IoT data mining
- Key-value Store (KVS)



Features

- Key length
  - ✧ 144/288/576/1152 bits
- Entry capacity
  - ✧ 1M entries / 288[bit] (*)
- **Search latency**
  - ✧ **10 cycles (on-chip memory mode)**
  - ✧ **TBD cycles (off-chip memory model)**
- Search speed
  - ✧ 150MSPS @150MHz
- Operations
  - ✧ Entry write/read/delete/update
  - ✧ Aging operations (optional)
- OpenFlow friendly
  - ✧ Field masking for N-tuple header field
  - ✧ Priority setting for every entry
- 28nm process silicon proven

(*) NOTE: Maximum capacity depends on target FPGA resource budget.

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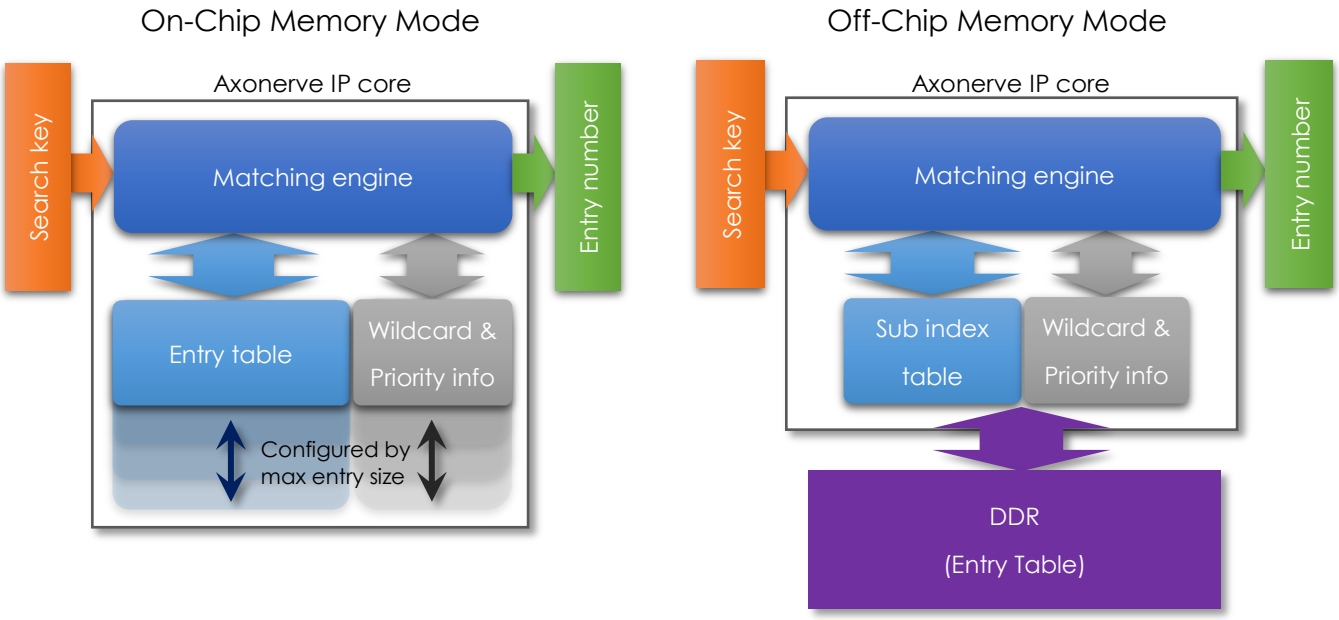
Operation Modes

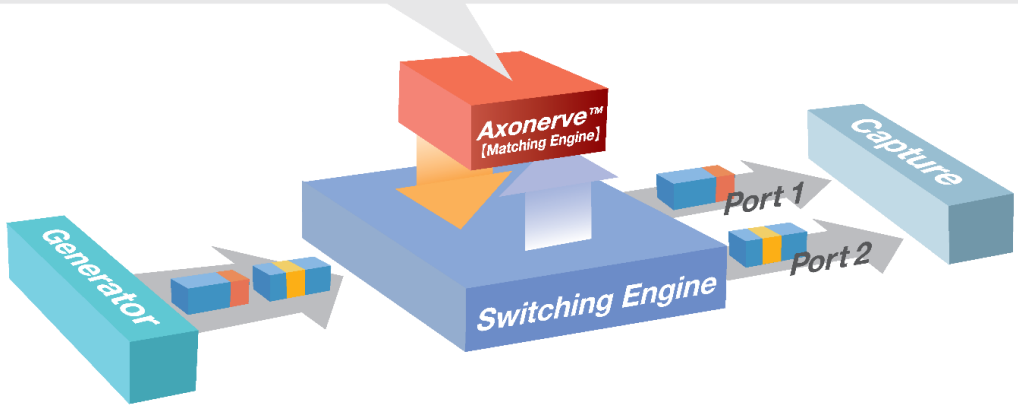


In on-chip memory mode Axonerve holds a whole entry table in FPGA, while in off-chip memory mode the entry table is placed in external memory devices and Axonerve holds only the indexes to the entry table and wildcard & priority infos in FPGA so that Axonerve can deal with more entries that cannot fit to FPGA internal memory.

Application Example (OpenFlow Switch)

Flow Table

Priority 6	MAC_SRC 48	MAC_DST 48	VLAN 12	IPV4_SRC 32	IPV4_DST 32	IP 8	TCP_SRC 16	TCP_DST 16	Action
100	*	*	*	192.168.10.100	*	6	22	*	<Action>
90	*	*	*	192.168.10.100	*	6	*	80	<Action>
80	*	*	*	192.168.10.0/24	192.168.1.100	6	*	*	<Action>
70	*	*	*	*	192.168.1.100	6	*	80	<Action>
60	*	*	*	*	192.168.1.100	6	*	*	<Action>
60	*	*	*	*	192.168.1.110	50	*	*	<Action>
50	*	*	*	*	10.0.0.0/16	*	*	*	<Action>
100	*	32:61:3C:4E:B6:05	1000	*	*	*	*	*	<Action>
50	*	32:61:3C:4E:A3:05	800	*	*	*	*	*	<Action>
50	*	32:61:3C:4E:A3:06	500	*	*	*	*	*	<Action>
50	32:61:3C:4E:A3:06	32:61:3C:4E:A3:06	*						<Action>



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