Longest Prefix Match (LPM) Engine for IPv4

Introduction

Axonerve is a next generation variant of the content-addressable memory (CAM) solution. Its unique algorithmic matching engine realizes high-speed & low-latency content matching at ultra-low power consumption.

Axonerve LPM IPv4 core can perform continuous longest prefix matching operation applicable to IPv4 address search with subnet masks from /8 to /32 with extremely low latency and achieve 150MSPS to track 100Gbps network packets.

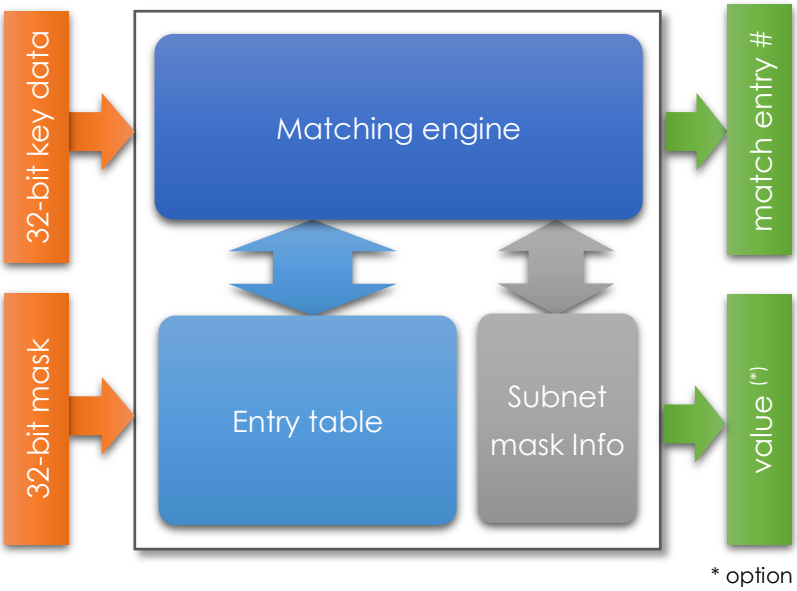
Axonerve is a fully-synthesizable IP core. It adopts common 6T-SRAM technology and requires no special memory structure design. It leads to power and area saving, and enables you to implement single or multiple instances of Axonerve IP cores in FPGA as well as ASIC.

Features

- Key length
  - ✧ 32 bits
- Entry capacity
  - ✧ ~1M entries (*)
- Search latency
  - ✧ 10 cycles (on-chip memory mode)
  - ✧ TBD cycles (off-chip memory mode)
- Search speed
  - ✧ ~150MSPS @150MHz
- Operations
  - ✧ Entry write/read/delete/update
  - ✧ Aging operations (optional)
- 28nm process silicon proven

(*) NOTE: Maximum capacity depends on target FPGA resource budget.

Axonerve IP core



* option

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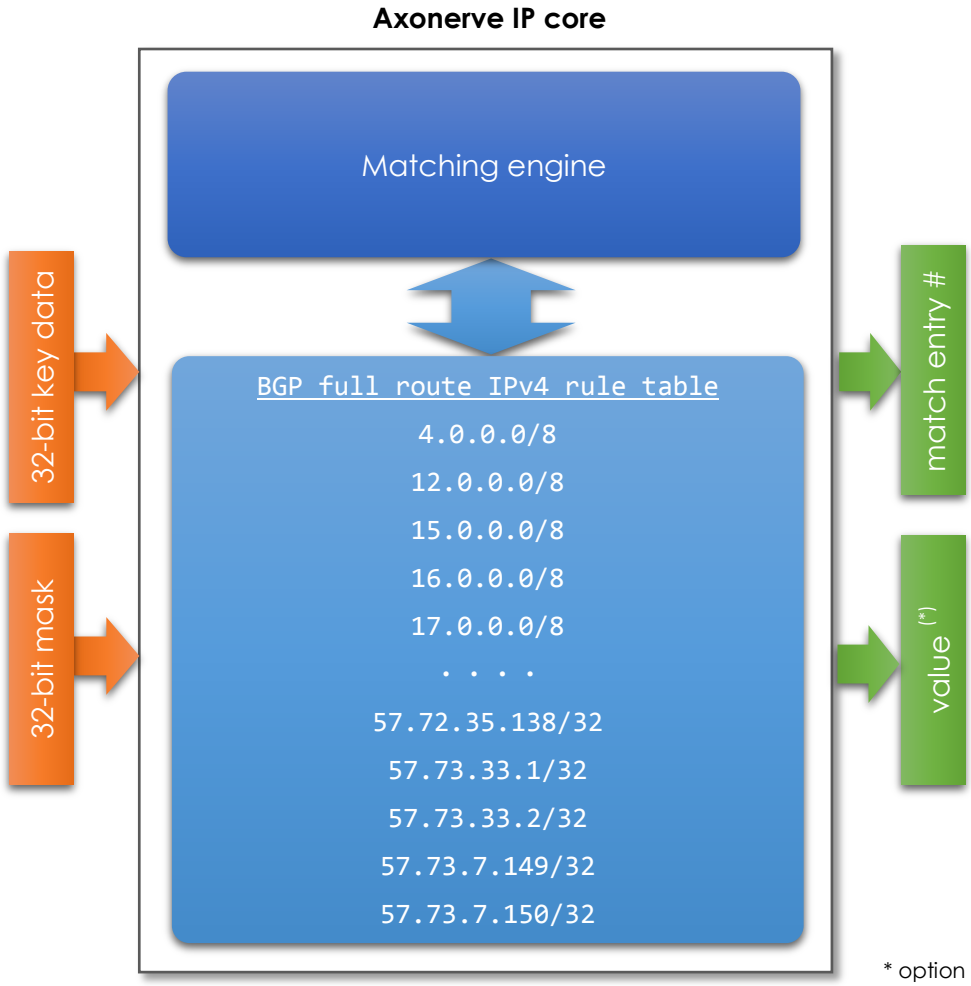
BGP IPv4 full route Matching Engine

BGP lookup solution

The BGP IPv4 full route Matching Engine is one of Axonerve solution products. It is a BGP full route dedicated search engine. The internal architecture and memory configuration is optimized for statistical characteristics of BGP full route rules, based on Axonerve LPM IPv4 IP core.

The BGP IPv4 full route Matching Engine can keep 0.5M+ IPv4 rules of BGP full route and continuously perform one lookup every clock cycle, which makes it possible for local Linux routers to offload BGP rule looking-up to the engine so as to realize 100G BGP routing.



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